Rahul Shrestha

Curriculum Vitae

Education

2009–2014 **Ph.D**, *Indian Institute of Technology Guwahati (VLSI Design Laboratory and National MEM Design Center)*, *Course-work CGPA – 9.18.*

2004–2008 **Bachelor of Engineering (Specialized in Telecommunication Engineering)**, *Visveswaraiah Technological University*, B. M. S. College of Engineering, Bangalore, *Percentage – 70.0 %.*
First Class

2001–2003 **Intermediate studies (Specialized in physics, chemistry, mathematics and computer-science)**, *Government of Karnataka Pre-university Education Board*, American Pre-university College, Bangalore, *Percentage – 75.5 %.*
First class

2001 **Xth standard**, *Indian Certificate of Secondary Education (ICSE) Board*, West Point School Darjeeling, *Percentage – 65.0 %.*
First Class

Work Experience

August-2014 **Assistant Professor**, *Center for VLSI and Embedded System Technologies (CVEST), International Institute of Information Technology Hyderabad (IIIT-H).*
Till date.

Research Interests

Areas

- Digital architecture of communication baseband and CMOS circuitry of analog RF section for the transceiver of cognitive-radio wireless sensors.
- Reconfigurable channel decoder for the next-generation of wireless communication.
- System on Chip (SoC) design and implementation of high-speed digital-architectures.
- Algorithmic aspects of error-correcting codes (Turbo and LDPC codes) and VLSI architectures of efficient channel-decoders.
- Application-Specific-Integrated-Circuits (ASIC) and Field-Programmable-Gate-Array (FPGA) implementations of digital/analog/mixed-signal designs.

PhD topic VLSI Design and Implementation of High-Throughput Turbo Decoder for Wireless Communication Systems.

Supervisor Prof. Roy P Paily.

Teaching Experience

Spring-2016 **Graduate Course in IIIT-Hyderabad**, VLSI Architectures.

Spring-2016 **Undergraduate Course in IIIT-Hyderabad**, Basic Electronics Laboratory.

Spring-2016 **Undergraduate Course in IIIT-Hyderabad**, Electronics Workshop - II.

Monsoon-2015 **Graduate Course in IIIT-Hyderabad**, Analog Mixed Signal Design.

Monsoon-2015 **Undergraduate Course in IIIT-Hyderabad**, Embedded Hardware Design.

Spring-2015 **Graduate Course in IIIT-Hyderabad**, VLSI Architectures.

Spring-2015 **Undergraduate Laboratory in IIIT-Hyderabad**, Electronics & Communication Laboratory.

2012 **Laboratory**, Worked as teaching assistant of digital IC design lab and electronics circuit design lab for M. Tech VLSI and B. Tech courses, respectively, in the Indian Institute of Technology Guwahati (IITG).

2011 **Laboratory**, Worked as teaching assistant of VLSI system design lab and analog circuit design lab for M. Tech VLSI course in the Indian Institute of Technology Guwahati (IITG).

2010 **Tutorial**, Conducted tutorial classes for electrical network analysis, basic electronics and electrical instrumentation courses for the first year B. Tech Students in the Indian Institute of Technology Guwahati (IITG).

Publications

Peer Reviewed Journals

- **Rahul Shrestha** and Roy Paily, "*Memory-Reduced Maximum-A-Posteriori-Probability Decoding for High-Throughput Parallel-Turbo Decoders*," **Journal of Circuits, Systems, and Signal Processing**, Volume: 35, Issue: 8, pp. 2832–2854, August-2016.
- Vijaya Kumar K, **Rahul Shrestha** and Roy Paily, "*Multi-Standard High-Throughput and Low-Power QC-LDPC Decoder for WiMAX and WiFi Standards*," **IET Circuits, Devices and Systems**, Volume: 10, Issue: 2, pp. 111–120, March-2016.
- **Rahul Shrestha** and Roy Paily, "*VLSI Design and Hardware Implementation of High-Speed Energy-Efficient Logarithmic-MAP Decoder*," **Journal of Low Power Electronics**, Volume: 11, Issue: 3, pp. 406–412, September-2015.
- Sachin Kumawat, **Rahul Shrestha**, Nikunj Daga and Roy Paily, "*High-Throughput LDPC-Decoder Architecture Using Efficient Comparison Techniques and Dynamic Multi-Frame Processing Schedule*," **IEEE Transactions on Circuits and Systems I: Regular Papers**, Volume: 62, Issue: 5, pp. 1421–1430, May-2015.
- **Rahul Shrestha** and Roy Paily, "*High-Throughput Turbo Decoder with Parallel Architecture for LTE Wireless Communication Standards*," **IEEE Transactions on Circuits and Systems I: Regular Papers**, Volume: 61, Issue: 9, pp. 2699–2710, September-2014.
- **Rahul Shrestha** and Roy Paily, "*Comparative Study of Simplified MAP Algorithms and an Implementation of Non-Parallel-Radix-2 Turbo Decoder*," **Journal of Signal Processing Systems**, Volume: 81, Issue: 2, pp. 305–320 , September-2014.
- **Rahul Shrestha** and Roy Paily, "*Performance and Throughput Analysis of Turbo Decoder for the Physical Layer of Digital-Video-Broadcasting-Satellite-Services-to-Handhelds (DVB-SH) Standard*," **IET Communications**, Volume: 7, Issue: 12, pp. 1211–1220, 2013.
- **Rahul Shrestha** and Roy Paily, "*Design and Implementation of a Linear Feedback Shift Register Interleaver for Turbo Decoding*," **Springer Berlin/Heidelberg Lecture Notes in Computer Science**, Volume: 7373, pp. 30–39, 2012.

International Conferences

- **Rahul Shrestha** and Roy Paily, "*Hardware Implementation of Max-Log-MAP Algorithm Based on Maclaurin Series for Turbo Decoder*," **IEEE International Conference on Communications and Signal Processing (ICCSP)**, pp. 509 - 511, 2011.
- **Rahul Shrestha** and Roy Paily, "*Design and Data Width Requirement for Fixed Point Turbo Decoders Based on Modified MAP algorithm*," **IEEE International Conference on Signal Processing and Communications (SPCOM)**, pp. 1 - 5, 2012.
- **Rahul Shrestha** and Roy Paily, "*Design and Implementation of a High Speed MAP Decoder Architecture for Turbo Decoding*," **26th IEEE International Conference on VLSI Design and the 12th International Conference on Embedded Systems (VLSID)**, pp. 86 - 91, 2013.
- **Rahul Shrestha** and Roy Paily, "*A Novel State Metric Normalization Technique for High-Throughput Maximum-a-Posteriori-Probability Decoder*," **IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI)**, pp. 903 - 907, 2013.
- **Rahul Shrestha** and Roy Paily, "*System Level Hardware Testing of a High Speed MAP Decoder Implemented on FPGA*," **IEEE International Conference on Signal Processing, Computing and Control (ISPCC)**, pp. 1 - 6, 2013.
- Vijaya Kumar K, **Rahul Shrestha** and Roy Paily, "*Design and Implementation of Multi-Rate LDPC Decoder for IEEE 802.16e Wireless Standard*," **IEEE International Conference on Green Computing, Communication and Electrical Engineering (ICGCCEE)**, pp. 1 - 5, 2014.
- **Rahul Shrestha** and Roy Paily, "*Hardware Implementation and Testing of Log-MAPP Decoder Based on Novel Un-Grouped Sliding-Window Technique*," **IEEE 5th International Symposium on Electronics System Design (ISED)**, pp. 171 - 175, 2014 (Best Paper Awarded).
- **Rahul Shrestha** and Utkarsh Rastogi, "*Design and Implementation of Area-Efficient and Low-Power Configurable Booth-Multiplier*," **29th IEEE International Conference on VLSI Design and the 15th International Conference on Embedded Systems (VLSID)**, pp. 599-600, January-2016.

Awards and Honors

2015 **Start-up Research Grants for Young Scientists**, Granted by Department of Science and Technology (DST) - Government of India, for the project entitled "ASIC Chip-Tapeout of Reconfigurable Multiple Radix Parallel-Turbo Decoder for Next-Generation Wireless-Communication Systems".

2014 **Winner**, of the Design Contest in 27th IEEE International Conference on VLSI Design and the 13th International Conference on Embedded Systems, for the work entitled "Hardware Implementation and Testing of LMAPP Decoder for High-Throughput Applications", held at the Indian Institute of Technology Bombay (IITB).

2012 **Reviewer**, "IEEE Transactions on Circuits and Systems I", "IEEE Transactions on Circuits and Systems II", "IEEE Transactions on VLSI Systems", "Integration, the VLSI Journals", "IET Circuits, Devices and Systems" and "IET Communications".

2012 **Membership**, Full member of IEEE technical society.

2011 **Fellowship at VLSID-2011**, Awarded fellowship by Indian Institute of Technology Madras to attain the tutorials and workshops at IEEE VLSID-2011 conference.

2009 **Graduate Aptitude Test Examination (GATE)**, Qualified GATE and cleared interview at Indian Institute of Technology Guwahati for admission in Ph.D program.

2006 **WIPRO Technology**, Placed in WIPRO Technology during the placement session in B. M. S College of Engineering Bangalore.

2004 **Karnataka Common Entrance Test (K-CET)**, Secured 525^{th} state rank in K-CET for engineering admission.

2002 **Table Tennis**, Held third position in inter college table tennis tournament in Bangalore.

2002 **Best Student Award**, Awarded by American Pre-unversity College Bangalore for academic excellence.

2000 **Table Tennis**, Winner of Darjeeling district level men's under-19 open table tennis tournament.

2000 **Blue Coat Holder of the year**, Awarded for the best all rounder student, by West Point School Darjeeling, with a full scholarship of one year.

1999 **Table Tennis**, Winner of inter ICSE-school table tennis tournament in B-division category.

Workshops Conducted

2014 **IEEE Workshop on MEMS and VLSI Digital Design Flow**, Organized by IEEE Student Branch, Indian Institute of Technology Guwahati.
February 08–09.

2014 **CADENCE Workshop - 2014, Schematic & Layout Design Flow in Cadence**, Organized by Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya (Shillong).
January 16–18.

2012 **INUP Familiarization Workshop on "Nanofabrication Technologies" for North-East Region, India**, Organized by Indian Institute of Science Bangalore in association with Indian Institute of Technology Guwahati.
September 28–29.

2011 **Digital Design - Functional Verification, Synthesis and RTL to GDS II flow using tools from *Cadence* and *Synopsys***, Organized by VLSI Design Lab. at Indian Institute of Technology Guwahati.
21–22 April.

Interest

Sports **Table tennis, foot ball, running, gym and trekking.**

Music **Indian classical, western blues and soft rock.**

Instrument **Guitar.**

Reading **Love to read while traveling.** *Favourite books: 'The Alchemist' and 'The Monk Who Sold His Ferrari'.*